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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,624	09/16/2003	Paul Murtagh	5646-114	1899
7590	09/13/2004			
Grant J. Scott Myers Bigel Sibley & Sajovec Post Office Box 37428 Raleigh, NC 27627			EXAMINER NGUYEN, LINH M	
			ART UNIT 2816	PAPER NUMBER

DATE MAILED: 09/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/663,624

Applicant(s)

MURTAGH, PAUL

Examiner

Linh M. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 16 September 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, 6, 7, 17 and 18 is/are rejected.
- 7) ☒ Claim(s) 2-5, 8-16, 19 and 20 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 09/16/03, 08/13/04.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### DETAILED ACTION

Claims 1-20 are presented in the instant application according to the Applicant's filing on 09/16/2003.

#### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

With regard to the rejection of claims 1, 6 and 17 under 35 U.S.C 112, first paragraph as being single means claims: This rejection is based on the language of M.P.E.P. section 2164.08(a) which discusses a rejection of a single means claim. This section of the manual states that a claim can be rejected as single means if a means covers every conceivable means for achieving the stated function. Claims 1, 6 and 17 are effectively single means claims because the only means that each claim recites to provide the lock condition is the "delay-locked loop". Even though each claim recites a feedback loop, this element is an inherent part of a "delay-locked loop". Thus, claims 1, 6 and 17 do not recite any means other than the "delay-locked loop" to perform the recited function. In other word, one skilled in the art would understand the claims to include a feedback loop, whether or not such were positively recited. Therefore, the claims are effectively single means claims. Note in *Fiers v. Sugano*, 984 F.2d 164, 25 USPQ2d

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1601 (Fed. Cir. 1993) which discusses situations analogous to single means or effectively single means claim.

Claims 2-5, 7-16 and 18-20 are also rejected under 35 U.S.C. 112, first paragraph because of their dependency on claim 1, claim 6 and claim 17, respectively.

Clarification is required.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 6-7 and 17-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Lu (U.S. Patent No. 6,100,735).

With respect to claim 1, Lu discloses, in Figures 1 and 7b-7c, an integrated circuit device comprising a delay-locked loop (DLL) [Fig. 1] that is configured to support transition from a partial feedback loop lock condition [Fig. 7b] to a full feedback loop lock condition [Fig. 7c] during a start-up time interval.

With respect to claim 6, Lu discloses, in Figures 1 and 7b-7c, an integrated circuit device comprising a delay-locked loop (DLL) [Fig. 1] that is configured to support a jump from a partial clock cycle lock condition [Fig. 7b] in a partial feedback loop to a two or more clock cycle lock condition [Fig. 7c] in a full feedback loop that comprises the partial feedback loop during a start-up time interval.

With respect to claim 7, Lu discloses, in Figures 1 and 7b-7c, a variable delay line

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that is responsive to a reference clock signal; and wherein the jump in lock condition is synchronized with the reference clock signal [ICLK].

With respect to claim 17, Lu discloses, in Figures 1-2 and 7b-7c, an integrated circuit device comprising a delay-locked loop (DLL) [Fig. 7] that is configured to support a jump from half or full clock cycle locking [Fig. 7b] of an auxiliary portion of a feedback loop to a two clock cycle locking [Fig. 7c] of a full portion of the feedback loop during a start-up time interval.

With respect to claim 18, Lu discloses, in Figures 1-2 and 7b-7c, a variable delay line that is responsive to a reference clock signal; and wherein the jump in lock condition is synchronized with the reference clock signal [ICLK].

***Allowable Subject Matter***

5. Claims 2-5, 8-16 and 19-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art on record does not show or fairly suggest:

A delay locked loop (DLL), which includes a variable delay line that is responsive to a reference clock signal; an auxiliary phase detector that is electrically coupled to the variable delay and a main phase detector that is responsive to the reference clock signal and a feedback clock signal, as called for in claims 2, 9, 12 and 19; and

A delay locked loop (DLL), which comprises a variable delay line and a fixed delay line that collectively define the full feedback loop, as called for in claim 8.

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*Citation of Relevant Prior Art*

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Brass et al. (U.S. Pub. No. 2003/0067334) discloses a circuit configuration for processing data having a control circuit for setting a phase or frequency relationship between two signals.

Prior art Stubbs et al. (U.S. Patent No. 6,727,739) discloses compensation for a delay locked loop.

*Inquiry*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Fri, Monday - Thursday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



**LINH MY NGUYEN  
PRIMARY EXAMINER**